



UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.ospto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,563	10/24/2001	Craig Hemsing	13158US02	5055
23446 7	7590 11/16/2004	<b>\$</b>	EXAM	INER
	WS HELD & MALLOY	Y, LTD	MOAZZAMI. NASSER G	
SUITE 3400	ADISON STREET		ART UNIT	PAPER NUMBER
CHICAGO, II	L 60661		2187	
			DATE MAILED: 11/16/2004	1 -4

Please find below and/or attached an Office communication concerning this application or proceeding.

			0.0			
1		Application No.	Applicant(s)			
		10/003,563	HEMSING ET AL.			
Office Action Sur	nmary	Examiner	Art Unit			
		Nasser G Moazzami	2187			
The MAILING DATE of the Period for Reply	is communication app	ears on the cover sheet with th	e correspondence address			
after SIX (6) MONTHS from the mailing do - If the period for reply specified above is le - If NO period for reply is specified above, the - Failure to reply within the set or extended	COMMUNICATION.  r the provisions of 37 CFR 1.13  ate of this communication.  ss than thirty (30) days, a reply  ne maximum statutory period v  period for reply will, by statute,  three months after the mailing	36(a). In no event, however, may a reply be within the statutory minimum of thirty (30) will apply and will expire SIX (6) MONTHS fr	timely filed  days will be considered timely.  om the mailing date of this communication.  NED (35 U.S.C. § 133).			
Status						
1) Responsive to communic	ation(s) filed on 24 O	ctober 2001.				
2a)☐ This action is <b>FINAL</b> .		action is non-final.				
• • • • • • • • • • • • • • • • • • • •	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Disposition of Claims						
4) ☐ Claim(s) <u>1-26</u> is/are pend 4a) Of the above claim(s) 5) ☐ Claim(s) is/are allowable 6) ☐ Claim(s) <u>1-26</u> is/are reject 7) ☐ Claim(s) is/are object 8) ☐ Claim(s) are subject	is/are withdrawwed. ted. ected to.	vn from consideration.				
Application Papers						
Replacement drawing sheet	October 2001 is/are: nat any objection to the office of the correction of the correc	a) $\square$ accepted or b) $\square$ object drawing(s) be held in abeyance. So in is required if the drawing(s) is	See 37 CFR 1.85(a). Objected to. See 37 CFR 1.121(d).			
Priority under 35 U.S.C. § 119						
a) All b) Some * c) 1. Certified copies of to 2. Certified copies of the certification from the	Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  a) All b) Some * c) None of:  1. Certified copies of the priority documents have been received.  2. Certified copies of the priority documents have been received in Application No					
Attachment(s)						
1) Notice of References Cited (PTO-892 2) Notice of Draftsperson's Patent Drawi 3) Information Disclosure Statement(s) (Paper No(s)/Mail Date	ng Review (PTO-948)	4) Interview Summa Paper No(s)/Mail 5) Notice of Informa 6) Other:				

Art Unit: 2187

## **DETAILED ACTION**

## Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 2. Claims 1-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Sherman et al. (U.S. Patent No. 5,175,830), hereinafter Sherman.

As per claim 1, Sherman discloses an apparatus for reducing the memory footprint of a first processor device, the apparatus comprising: a segment of program code which is split into portions including at least one controlling piece and at least one separate working piece; a storage area for storing certain pieces of the program code; a first memory area associated with the first processor device for receiving certain portions of the program code; and a hardware transfer mechanism for efficiently linking the storage area with the first memory area, wherein the memory footprint of the first processor device is reduced by locating certain controlling pieces of the program code in the storage area, and transferring only certain working pieces of the program code in the first memory area [differentiating overlay into a code portion and a data portion, storing the data portions within the firs memory and the code portions

Art Unit: 2187

within a second memory (column 1, lines 65-67); allocating a code area and data area within main memory and storing the data and code portions within the allocated areas (column 2, lines 6-27); a load and control system determines which program or overlays stored on a mass storage and are to be loaded in support of a particular application program being run (column 3, lines 38-60)].

As per claims 2-12, Sherman teaches that the storage area includes a second memory area associated with second processor device [controller for accessing the disk 9 (see Fig. 2)]; Sherman further discloses first and second memories and swapping a required code portion from the second memory into the first memory for execution by the CPU; a load and control system for determining which program or overlays to be loaded from the mass storage in support of a particular program being run and copying the stored and relocated code portion to the expanded memory [column1, line 65 through column 2, line 27; column 3, lines 38-50; and it is inherent in the art that the mass storage is a low cost memory than the main memory].

As per claims 13-26, claims 13-26 encompass the same scope of the invention as those of claims 1-12 in addition of performing the steps method and some units for performing the functions. Therefore, claims 13-26 are rejected for the same reasons as stated above with respect to claims 1-12.

Page 4

Art Unit: 2187

3. Claim 26 is rejected under 35 U.S.C. 102(e) as being anticipated by Chin et al (U.S. Patent No. 6,608,625) or Jacobs et al. (U.S. Patent No. 6,385,678).

As per claim 26, Chin or Jacob teach a processing unit having a cache memory; and SDRAM; and an arbiter configured to exchange code and data between the SDRAM and the cache memory [for chin's patent see column 12, line 59 through column 13, line 57; and for Jacob's patent see column 3, line 61 through column 4, line 7].

## Conclusion

- 4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.
- 5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nasser G Moazzami whose telephone number is (571) 272-4195. The examiner can normally be reached on 7:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2187

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Page 5

NASSER MOAZZAMI PRIMARY EXAMINES

11/15/2004